Web Results 1 - 1 of 1 for "unit interval" "delay line" tap "delay clock" "active edge". (0.30 seconds)

Data receiver with servo controlled delayed clock invention
A Time Ruler is used to periodically discover the Unit Interval (UI) for a ... will clock any far-to-the-right ZEROs in the tapped delay line into SZERO, ...
www.freshpatents.com/Data-receiver-with-servo-controlled-delayed-clock-dt20051006ptan20050220236.php?type... - 60k - Cached - Similar pages - Note this

Web Results 1 - 3 of 3 for "unit interval" "delay line" tap "delay clock" active edge. (0.25 seconds)

Data receiver with servo controlled delayed clock invention
Assuming that the active edge of a bus signal is the rising edge, ... in the data will clock any far-to-the-right ZEROs in the tapped delay line into SZERO, ...
www.freshpatents.com/Data-receiver-with-servo-controlled-delayed-clock-dt20051006ptan20050220236.php?type .. - 60k - Cached - Similar pages - Note this

[PDF] Xilinx XAPP462 Using Digital Clock Managers (DCMs) in Spartan-3 ...
File Format: PDF/Adobe Acrobat - View as HTML
The minimum delay-line tap resolution, listed as the DCM_TAP_MIN ..... only relevant on the active clock edge. For example, in single-data rate (SDR) ...
duteela.et.tudelft.nl/~elca/XilinxTutor/documents/xapp462.pdf - Similar pages - Note this

[PDF] DS110: "Virtex-II Pro X Platform FPGAs: Advance Product Specification"
File Format: PDF/Adobe Acrobat
The falling clock edge option uses the BUFGCE_1. and BUFGMUX_1 primitives. BUFGCE. If the CE input is active (High) prior to the incoming rising ...
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IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

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1. Instantaneous Clockless Data Recovery and Demultiplexing
Analui, B.; Hajimiri, A.;
Circuits and Systems II: Express Briefs, IEEE Transactions on [see also Circu and Digital Signal Processing, IEEE Transactions on]
Volume 52, Issue 8, Aug. 2005 Page(s):437 - 441
Digital Object Identifier 10.1109/TCSII.2005.850453
AbstractPlus | Full Text: PDF(592 KB) IEEE JNL
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1. Positioning the active edge of a clock signal
Wood, Glenn (Agilent Technologies, Inc.(US-DELAWARE)), *UNITED KINGDOM PATENT APPLICATION*, Oct 2005
patno:GB2412829
...to keep its active edge in the middle...delays the clock is responsive...adjusted clock delay is maintained until active servoing can...to half the unit interval A bank of XOR...the tapped delay line. That number...additional data delay lines, and...the drift in clock phase teeing corrected...discovering Unit Interval using a Time...positioning the active edge of a clock...
Full text available at patent office. For more in-depth searching go to LexisNexis
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2. RE-TIMER CIRCUIT FOR DATA RECOVERY WITH FAST RECOVERY FROM A LOW POWER MODE
ABROSIMOV, Igor Anatolievich, *PATENT COOPERATION TREATY APPLICATION*, Feb 2006
patno:WO06011830
...the re- sampling clock, a tracking pipeline...positioning of the edge of the re-sampling...selector comprises a delay line for generating delayed...outputs from the delay line; a third data...input a reference clock, the delay line...of stages in the delay line, preferably the...inputs to select one tap from the delay line, preferably the...
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1. Positioning the active edge of a clock signal
Wood, Glenn (Agilent Technologies, Inc.(US-DELAWARE)), *UNITED KINGDOM PATENT APPLICATION*, Oct 2005
patno:GB2412829
...location ofthe active edge ofthe clock. The result...to a clock delay circuit to...incorporated UNIT INTERVAL DISCOVERY...tapped data delay line, going from...least one unit interval. The various...taps of the delay line for an isolated...
Full text available at patent office. For more in-depth searching go to LexisNexis
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2. Stratix GX Transceiver User Guide [PDF-8MB]
Jan 2005
..... 2–12 Clock Recovery
Unit .....
[http://www.altera.com/literature/ug/ug_sgx.pdf]
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3. RE-TIMER CIRCUIT FOR DATA RECOVERY WITH FAST RECOVERY FROM A LOW POWER MODE
ABROSIMOV, Igor Anatolievich, *PATENT COOPERATION TREATY APPLICATION*, Feb 2006
patno:WO06011830
...the re- sampling clock, a tracking pipeline...positioning of the edge of the re-sampling...selector comprises a delay line for generating delayed...outputs from the delay line; a third data...input a reference clock, the delay line...of stages in the delay line, preferably the...inputs to select one tap from the delay line, preferably the...
Full text available at patent office. For more in-depth searching go to LexisNexis
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4. EEmmbbeedddeedd LLooww--PPoowweerr WWiirreelleessss SSeennssoorr... [PDF-5MB]
May 2001
...73 7 Sampling Clock Requirements...95 9 8.3.2 Clock Recovery...Figure 3. Jitter is when the sampling clock edge's location changes over time [8, see...
[http://www.media.mit.edu/resenv/pubs/theses/ZOE_MEng_T...]
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5. DS083: "Virtex-II Pro™ Platform FPGAs: Advance Product Specification" [PDF-3MB]
Mar 2003
...configuration - Active Interconnect...High-performance clock management...16 global

clock multiplexer...all parts • Active Interconnect...predictable routing delay, independent...The leading-edge 0.13 µm CMOS...and leading-edge I/O standards...Digital Clock Manager (DCM...distribution delay compensation...fine-grained clock phase shifting. A...resources called Active Interconnect... [http://www.physics.ohio-state.edu/~cms/cfeb/datasheets...]
similar results

6. DS083: "Virtex-II Pro Platform FPGAs: Advance Product Specification" [PDF-3MB]
Feb 2005
...Multipliers - Global Clock Multiplexer...configuration - Active Interconnect...16 global clock multiplexer...all parts • Active Interconnect...predictable routing delay, independent...The leading-edge 0.13 µm CMOS...and leading-edge I/O standards...Digital Clock Manager (DCM...distribution delay compensation...fine-grained clock phase shifting. A...resources called Active Interconnect... [http://courses.ece.uiuc.edu/ece412/References/XUP/virt...]
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7. DS083: "Virtex-II Pro™ Platform FPGAs: Advance Product Specification" [PDF-3MB]
Jul 2003
...configuration - Active Interconnect...High-performance clock management...16 global clock multiplexer...all parts • Active Interconnect...predictable routing delay, independent...The leading-edge 0.13 µm CMOS...and leading-edge I/O standards...Digital Clock Manager (DCM...distribution delay compensation...fine-grained clock phase shifting. A...resources called Active Interconnect... [http://www.ee.ucla.edu/~herwin/ocdma/afx-300/ds083.pdf]
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8. A 10-Gb/s two-dimensional eye-opening monitor in 0.13-/spl mu/m standard CMOS
Analui, Behnam / Rylyakov, Alexander / Rylov, Sergey / Meghelli, Mounir / Hajimiri, Ali, *article*, Dec 2005
...lines, i.e., LC networks [3]–[5] or active delay elements [6]. At multigigabit per second data rates, the passive or active delay cells become more sensitive to on-chip...optimizes the phase of the retiming clock. Eye-opening monitor circuits have also...input common mode and . Every positive edge on next_ref triggers a reference-set...
Full text available from Caltech
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9. Amplitude monitor for high-speed signals
Farjad-rad, Ramin, *UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT PUBLICATION*, Jun 2006
patno:US20060140318
...next falling edge of sample clock Sclk. Due...an N-stage delay line 700, an embodiment...eight-stage delay line 520 of FIG...tenth of the unit interval (i.e. 0.1...selectable delay line 810, a three-bit...each sample-clock phase, as detailed...
Full text available at patent office. For more in-depth searching go to LexisNexis
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10. DS110: "Virtex-II Pro Platform FPGAs: Advance Product Specification" [PDF-607K]
Dec 2003
...Width 1 byte 1:2(1) N/A 2 byte 1:1 N/A 4 byte 2:1(1) 1:1 8 byte N/A 2:1(1) Notes: 1. Each edge of slower clock must align with falling edge of faster clock. Virtex-II Pro X™ Platform FPGAs: Functional Description R DS110-2 (v1.0) November 17... [http://homepages.fh-regensburg.de/~grf39054/unterlagen...]
similar results

11. Microsoft Word - JTC1_COVER.doc [PDF-4MB]
Dec 2005
... . 104 10.3.2 Signal edge models . . . . . 104 10.3.3.... . . . . 112 10.5.2 Jitter measurements with a "bit clock" (level 1) . . . . . 113 10.5.3 Jitter measurements with a "pattern... [http://www.t10.org/ftp/t11/document.05/05-870v0.pdf]
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12. MJSQ [PDF-3MB]
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13. a; Abbreviation for atto (10-18). See metric system, abandoned call;... [2MB]
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...location without the use of an intermediate reference, e.g., a base address or a relative address. [After Weik '96] absolute delay: 1. The time interval or phase difference between transmission and reception of a signal. 2. The total time between the instant...
[http://www.its.bldrdoc.gov/projects/devglossary/alldef...]
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14. Implementing High-Performance DSP Functions in Stratix & Stratix GX Devices, Stratix GX Device Handbook, Volume 2, Chapter 19 [PDF-2MB]
Feb 2005
...reuse the same hardware. Consider the 8-tap filter shown in Figure 19–2. The TDM...with a TDM factor of 2. A 2×-multiplied clock is required to run the filter. On cycle...stored in a register. On cycle 1 of the 2× clock, the user loads the remaining four coefficients...multipliers to achieve the functionality of an 8-tap filter. Thus, TDM is a good way to save...the multipliers can run at n- times the clock speed. The coefficients can be stored...
[http://www.altera.com/literature/hb/sgx/ch_7_vol_2.pdf]
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15. Stratix GX Device Handbook, Volume 2 [PDF-10MB]
Jun 2006
..... 2–12 Clock Recovery Unit .....
[http://www.altera.com/literature/hb/sgx/sgx_v2.pdf]
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16. MJSQ [PDF-4MB]
Dec 2005
...104 10.3.2 Signal edge models...112 10.5.2 Jitter measurements with a "bit clock" (level 1...114 10.5.4 Jitter measurements with 'no clock and no marker' (level 2...
[http://www.t10.org/ftp/t11/document.05/05-858v0.pdf]
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17. MJSQ [PDF-3MB]
Oct 2005
...interoperability and signal margin specifications for SAN applications, use of adaptive or predictive compensation schemes implemented in active elements or ports, and higher speed at longer distance. The goals of this technical report are: • To define and describe the...
[http://www.t11.org/ftp/t11/pub/fc/mjsq/04-101v5.pdf]
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18. MJSQ [PDF-3MB]
Jun 2004
...interoperability and signal margin specifications for SAN applications, use of adaptive or predictive compensation schemes implemented in active elements or ports, and higher speed at longer distance. The goals of this technical report are: • To define and describe the...
[http://www.t11.org/ftp/t11/pub/fc/mjsq/04-101v4.pdf]
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19. MJSQ [PDF-3MB]
May 2004
...specifications for SAN applications, increased interest in using adap- tive or predictive compensation schemes implemented in active elements or ports, and higher speed at

longer distance. The goals of this technical report are: • To define and describe the... [http://www.t11.org/ftp/t11/pub/fc/mjsq/04-101v2.pdf]
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...specifications for SAN applications, increased interest in using adap- tive or predictive compensation schemes implemented in active elements or ports, and higher speed at longer distance. The goals of this technical report are: • To define and describe the... [http://www.t11.org/ftp/t11/pub/fc/mjsq/04-101v1.pdf]
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Application Number Information

Application Number: 10/815156
Assignments

Examiner Number: 80488 / TORRES, JUAN

Filing or 371(c) Date: 03/31/2004 eDan

Group Art Unit: 2611 IFW Madras

Effective Date: 03/31/2004

Class/Subclass: 375/355.000

Application Received: 04/01/2004

Lost Case: NO

Pat. Num./Pub. Num: /20050220236

Interference Number:

Issue Date: 00/00/0000

Unmatched Petition: NO

Date of Abandonment: 00/00/0000

L&R Code: Secrecy Code:1

Attorney Docket Number: 10020213-1

Third Level Review: NO

Secrecy Order: NO

Status: 77 /RESPONSE TO EX PARTE QUAYLE ACTION ENTERED AND FORWARDED TO EXAMINER

Status Date: 01/02/2008

Confirmation Number: 8199

Oral Hearing: NO

Title of Invention: DATA RECEIVER WITH SERVO CONTROLLED DELAYED CLOCK

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Inventor Information for 10/815156

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